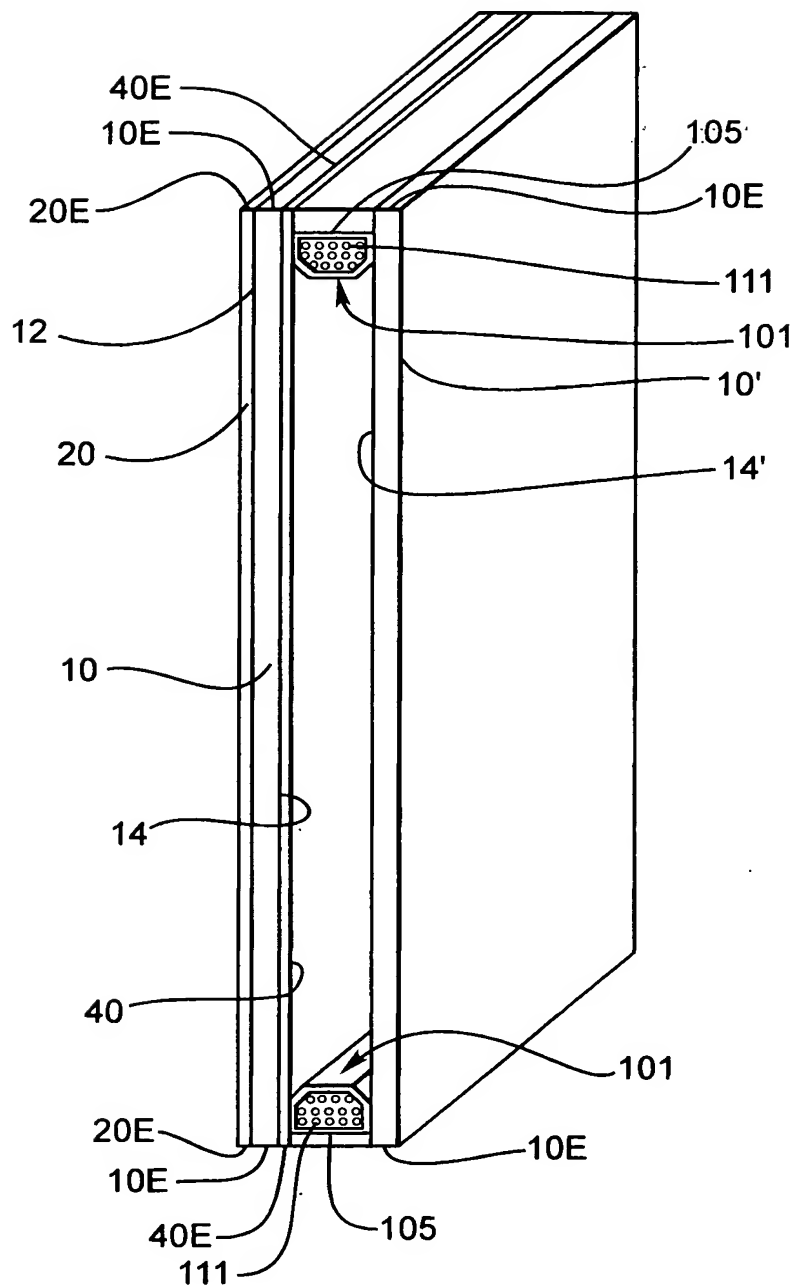
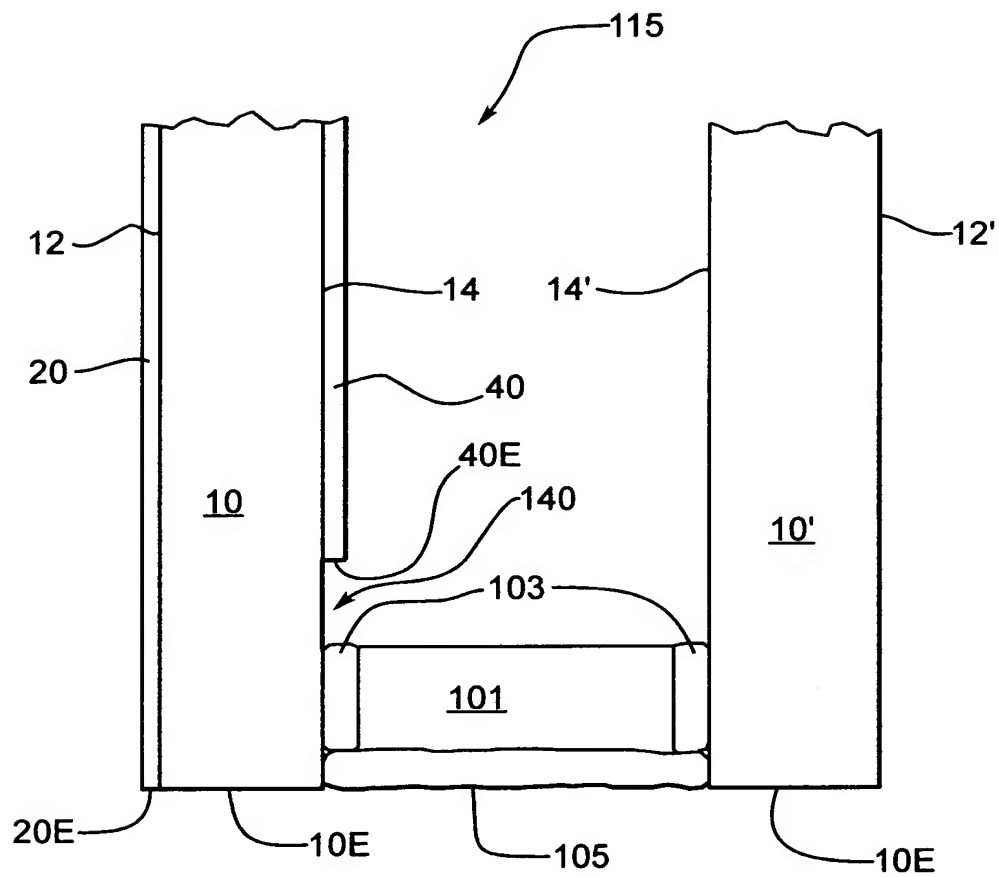




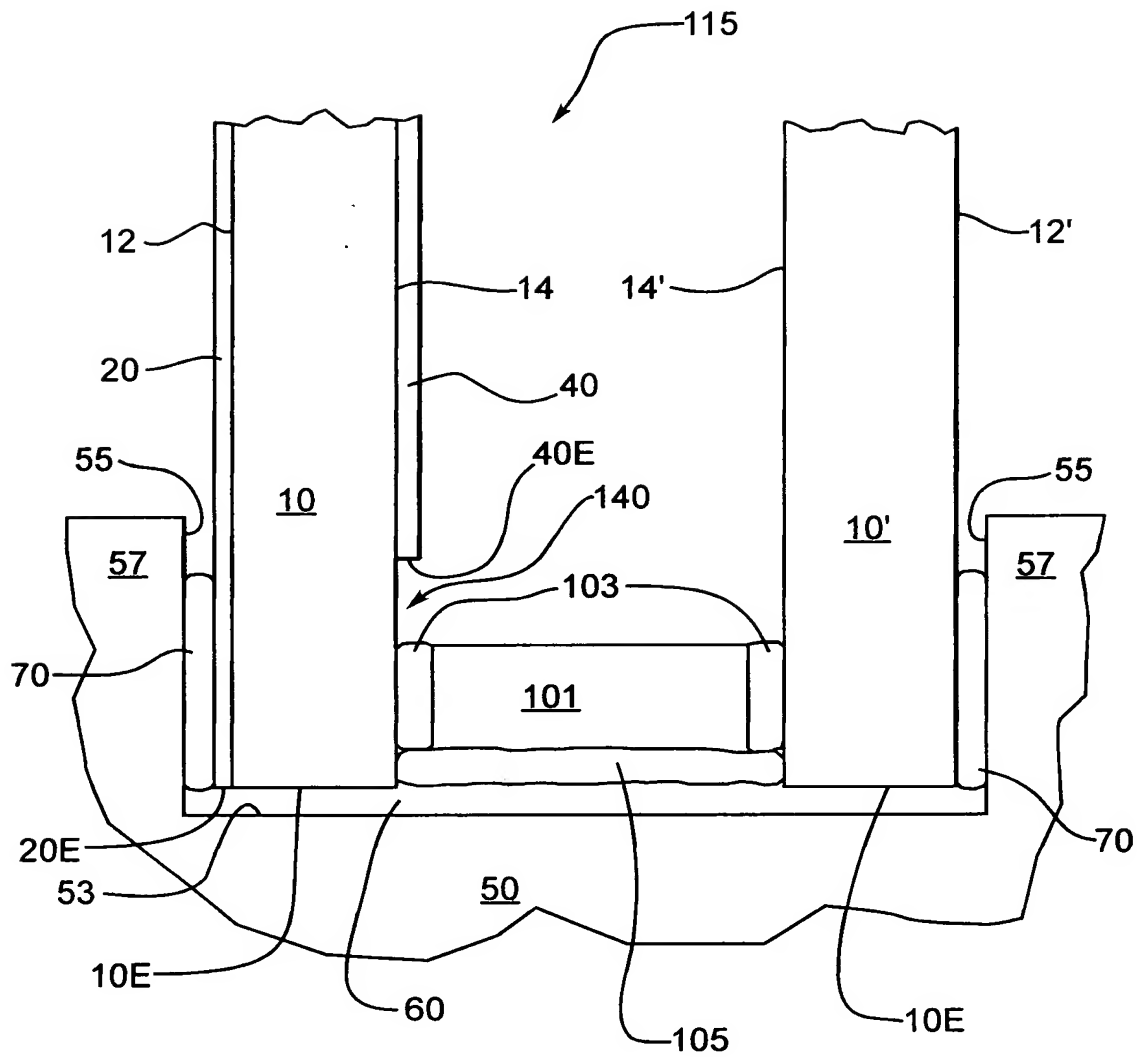
*Fig. 1*



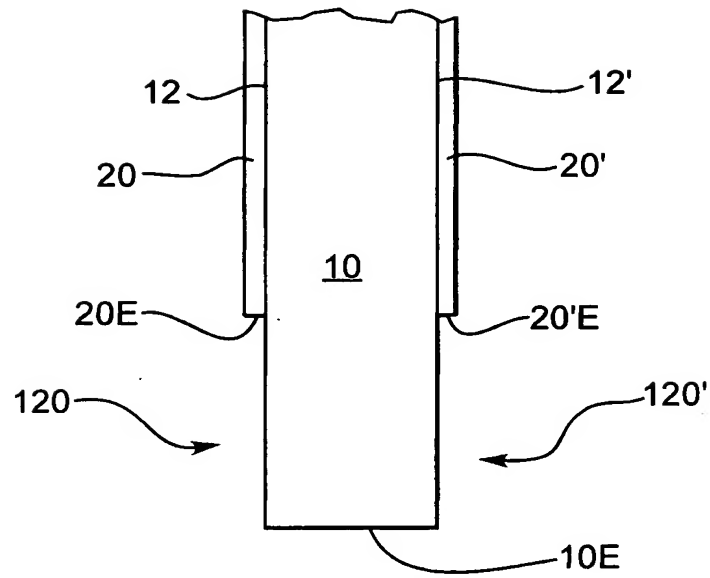
*Fig. 2*



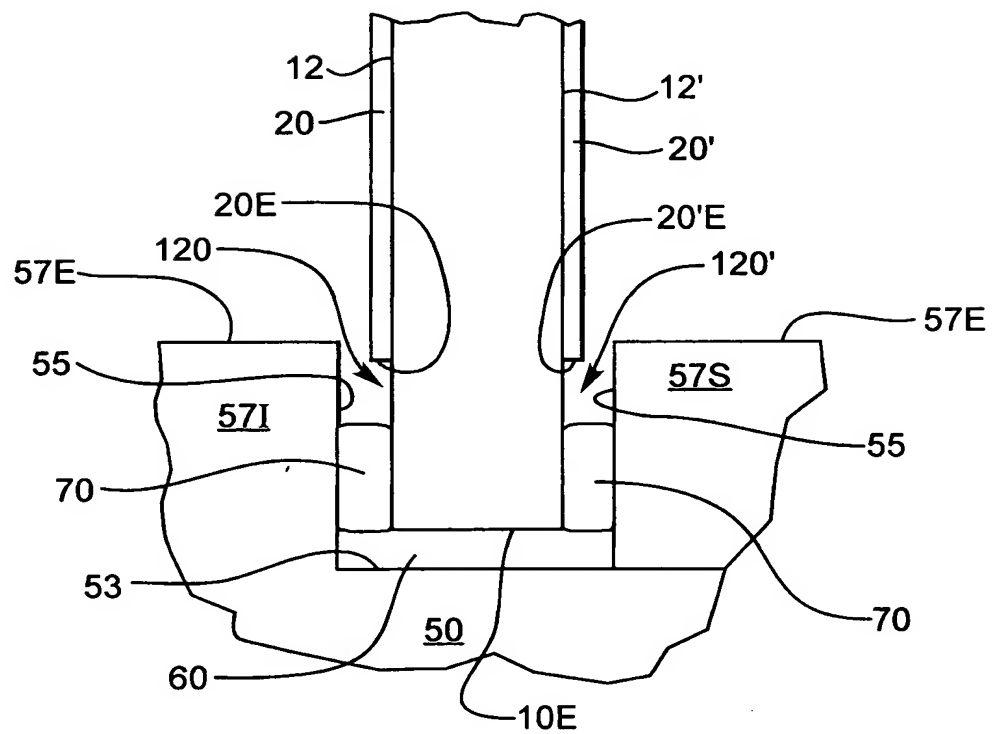
*Fig. 3*



*Fig. 4*

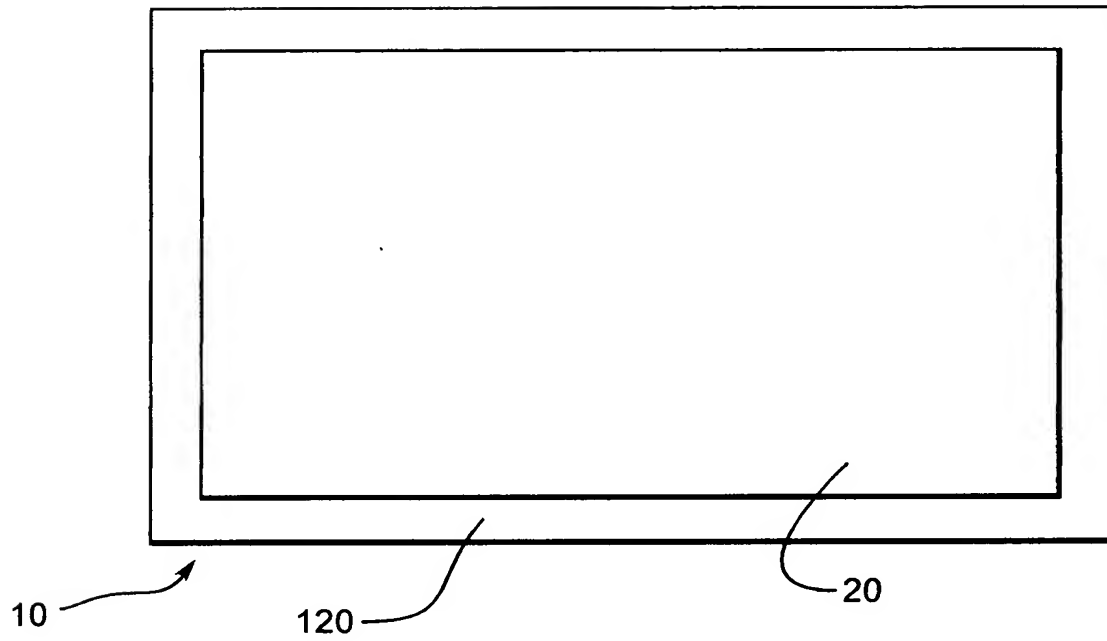


*Fig. 5*

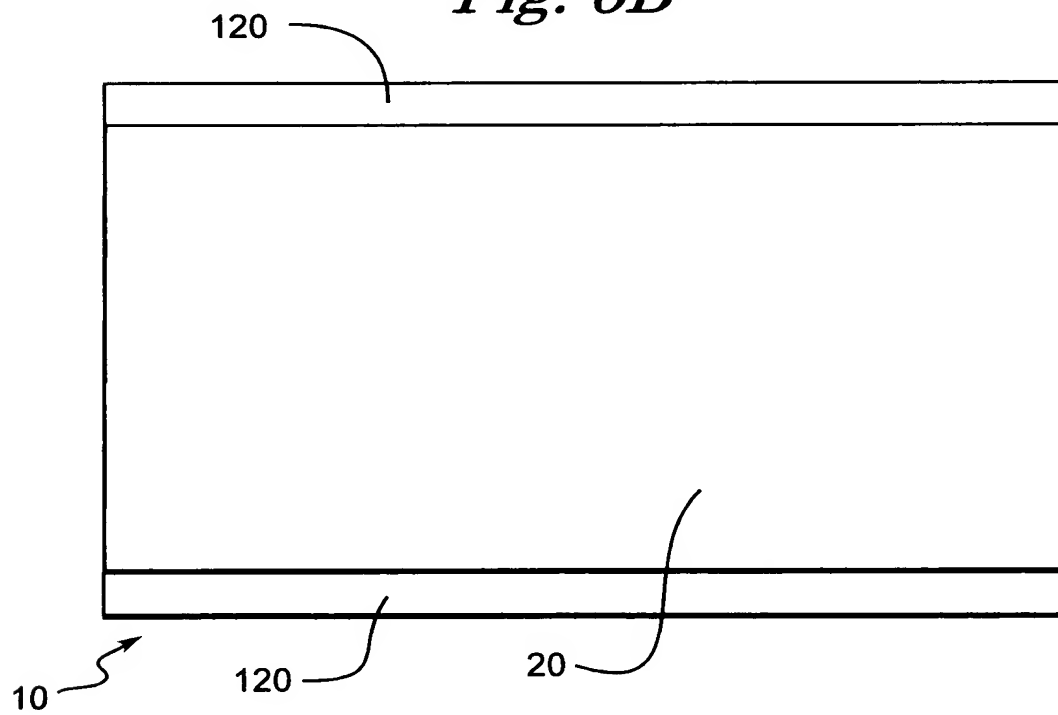




*Fig. 6A*

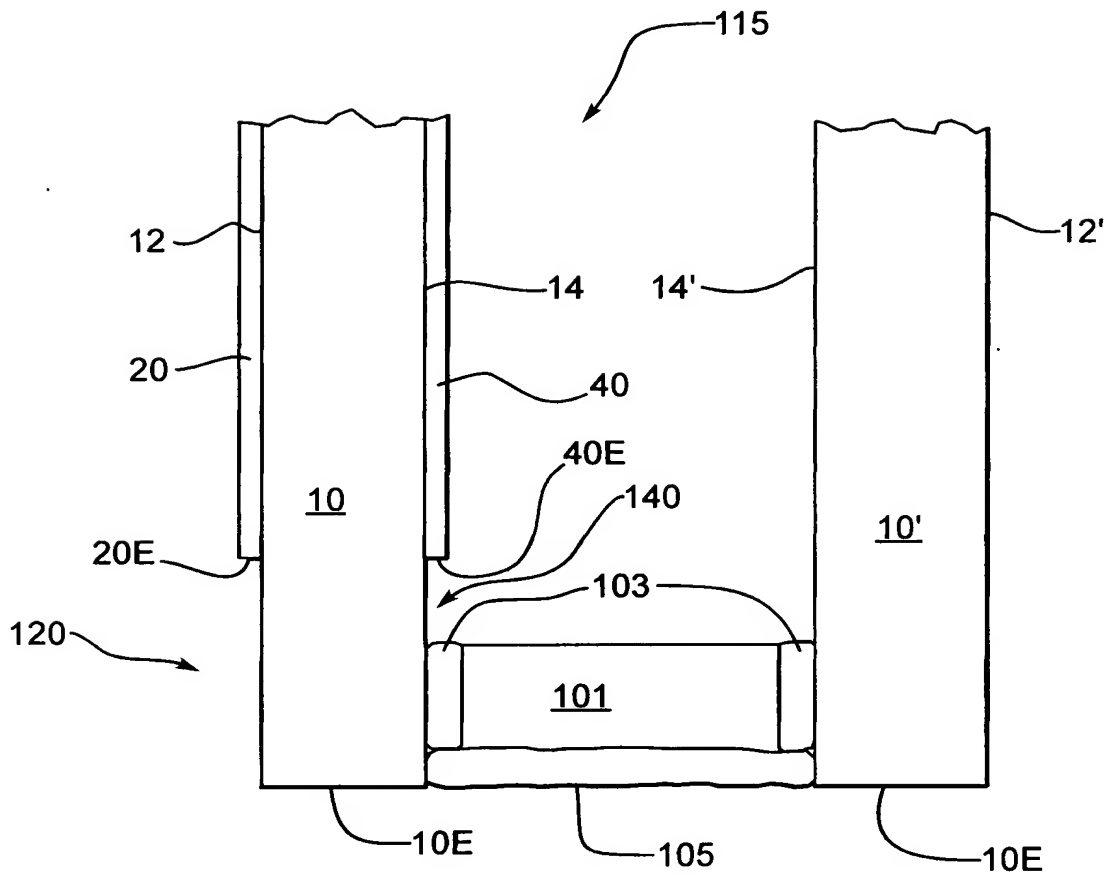


*Fig. 6B*

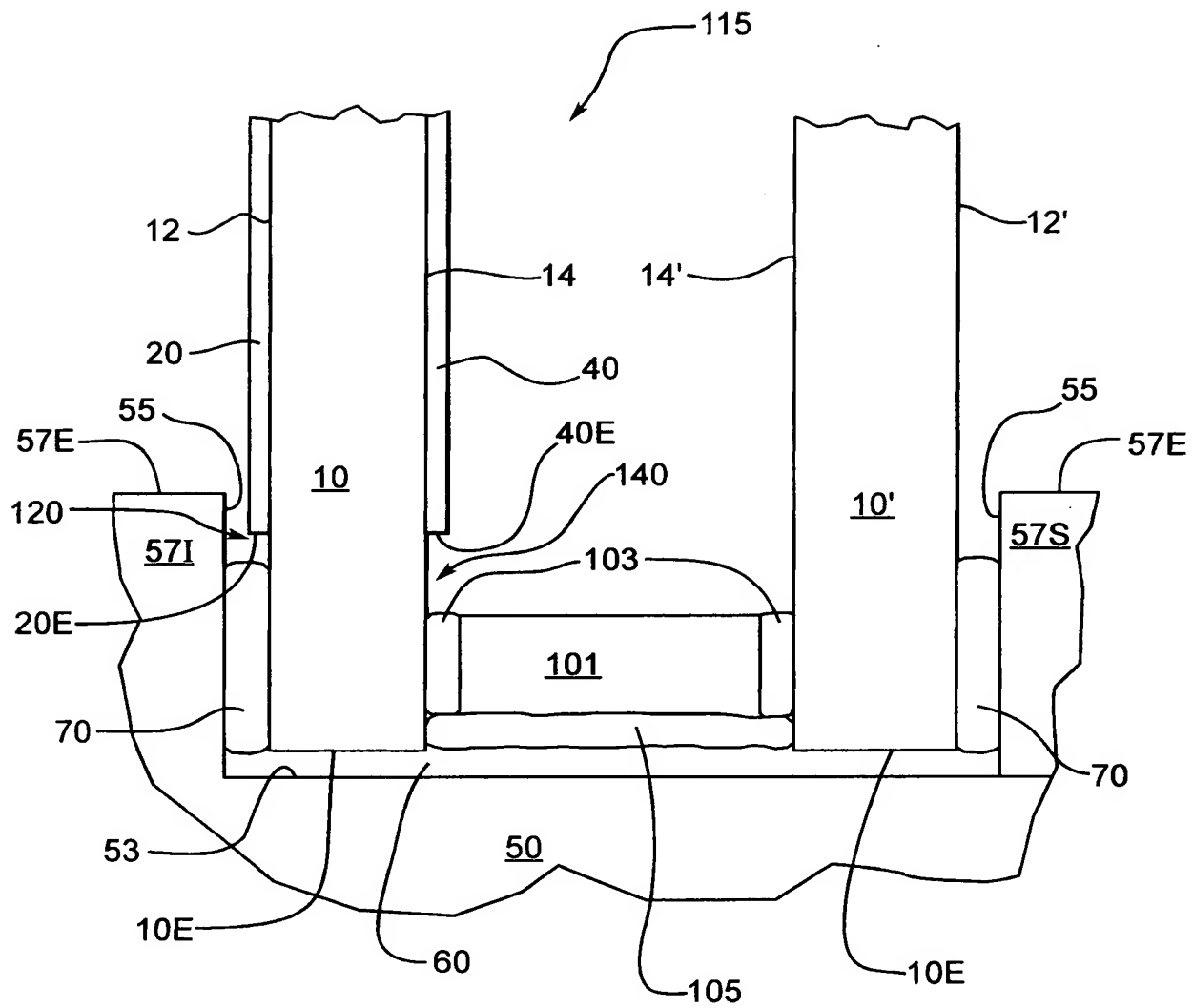




*Fig. 7*

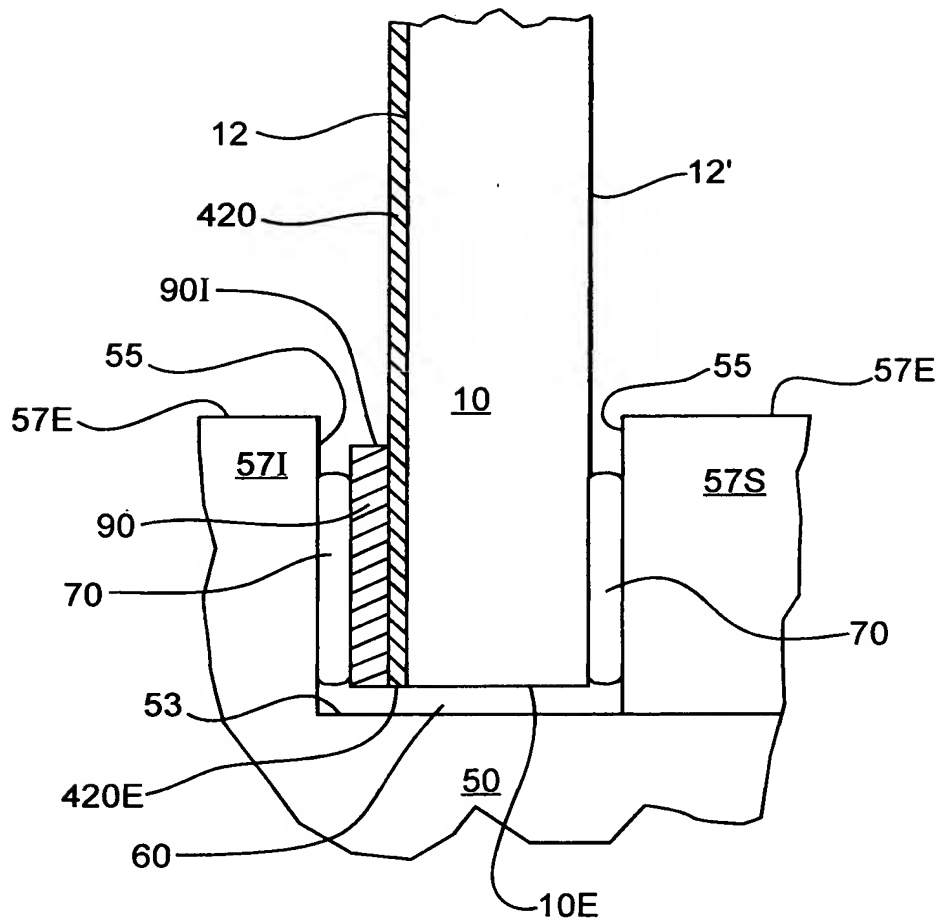


*Fig. 8*



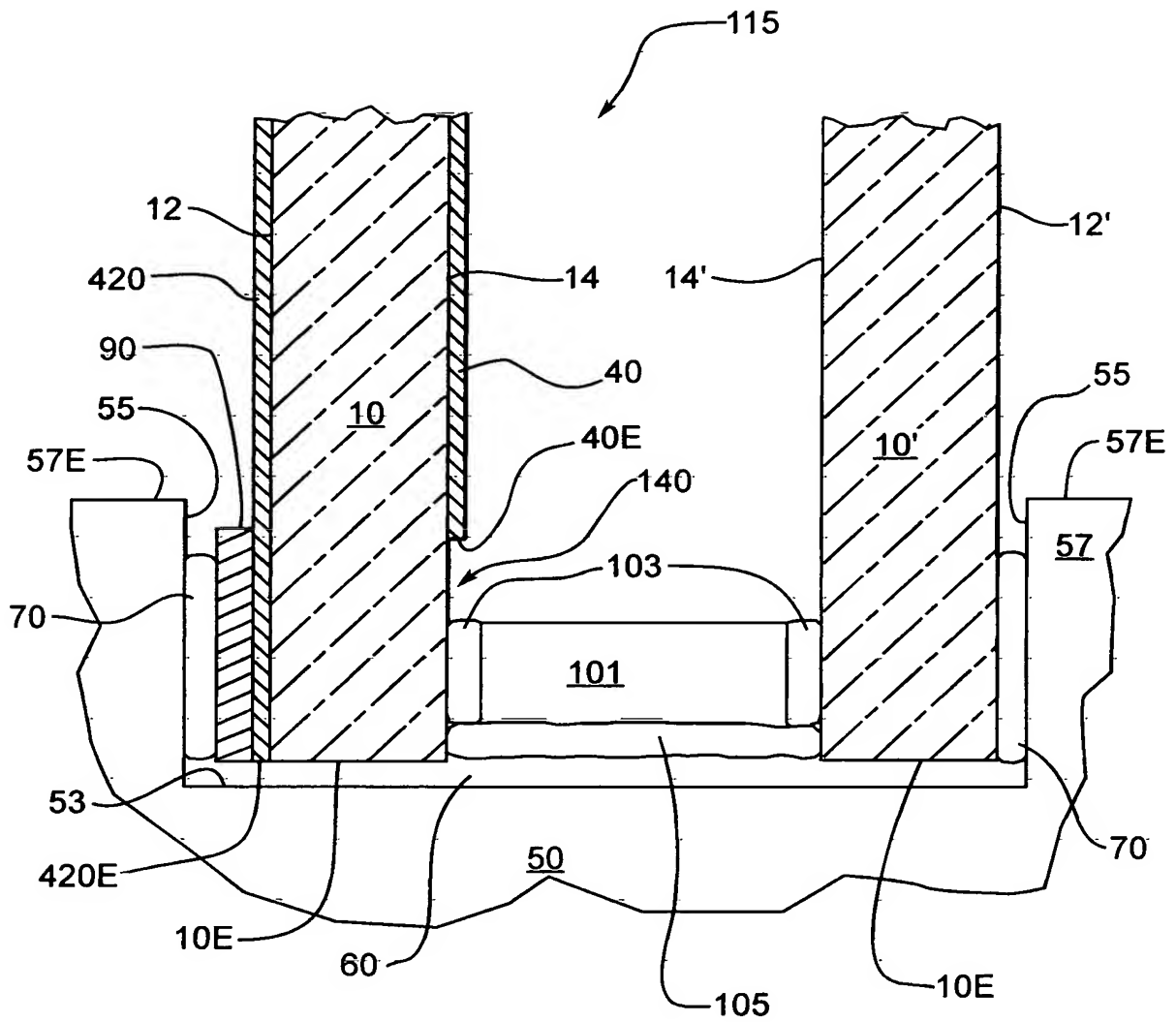


*Fig. 9*



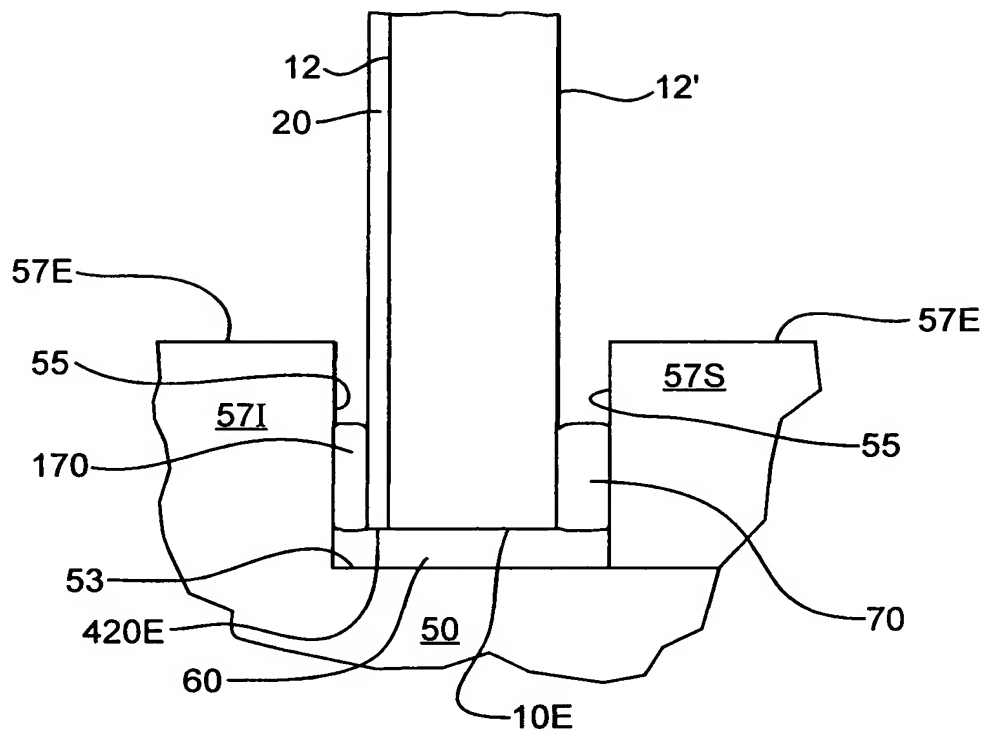


*Fig. 10*





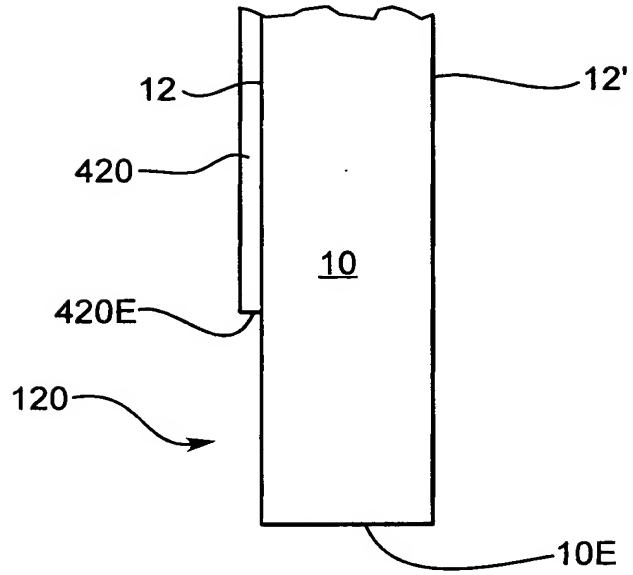
*Fig. 11*



A cross-sectional view of a semiconductor device 115. The device features a central substrate 10 with a top surface 12 and a bottom surface 10E. A layer 14 is disposed on the top surface 12, and a layer 14' is disposed on the bottom surface 10E. A central region 101 is defined within the substrate 10, and a layer 103 is disposed on its top surface. A layer 40 is disposed on the top surface 12, and a layer 420 is disposed on the bottom surface 10E. A layer 50 is disposed on the bottom surface 10E, and a layer 60 is disposed on the top surface 12. A layer 70 is disposed on the bottom surface 10E, and a layer 53 is disposed on the top surface 12. A layer 55 is disposed on the top surface 12, and a layer 57E is disposed on the bottom surface 10E. A layer 57I is disposed on the top surface 12, and a layer 57S is disposed on the bottom surface 10E. A layer 170 is disposed on the top surface 12, and a layer 105 is disposed on the bottom surface 10E.



*Fig. 13*





*Fig. 14*

